# SD2421
# Loop Powered 4-20mA DAC

## Features

- 4-20mA current output
- 16 bits resolution and monotonicity
- ±0.01% integral nonlinearity
- 3V/3.3V/5V selectable voltage source
- 2.5V and 1.25V precision reference
- 520uA maximum quiescent current
- HART® compatible
- Flexible serial interface
- Flexible alarm current output
- Short circuit protection and over current protection
- 16 pins SOIC packages
- -40℃ to +85℃ operating range

## General Description

The SD2421 is a complete 4-20mA loop powered DAC which converts digital signal into current. Its large scale integration, high precision, and low cost design is specifically well suited for smart 4-20mA transmitter manufacturer in the industrial control area.

The DAC uses Σ-Δ architecture. It guarantees 16 bits resolution and monotonicity, and ±0.01% integral nonlinearity. The IC provides 4mA zero scale output current (±0.02% FS error), and 20mA full scale output current (±0.1% FS error). Full scale setup time to ±0.1% is less than 8ms.

The SD2421 has a built-in voltage regulator that can be set to 3V, 3.3V, or 5V through different pin connections. The IC also has built-in 2.5V and 1.25V precision voltage references. Both regulator and precision references are used by the IC itself, and can also be used by other devices in the transmitter system. Thus, there is no need for standalone regulator or precision reference. However, a pass transistor is required in order to extend the loop operating voltage range. Together with this transistor, the SD2421 system can work from VCC+2V to the transistor's breakdown voltage.

The SD2421 can work together with HART or other similar FSK protocols without affecting the IC's own performance. It communicates to microcontroller through three serial ports. The simple scheme can operate up to 3Mbps.

The SD2421 has programmable alarm current function that can send out of range current to indicate malfunction.

There is built-in short circuit protect between COM and LOOPRTN, and over current protection between BOOST and LOOPRTN.

## Ordering Information

| Package | Part Number |
|---|---|
| SOP16（wide body） | SD2421A |

## Pin Diagram and Descriptions

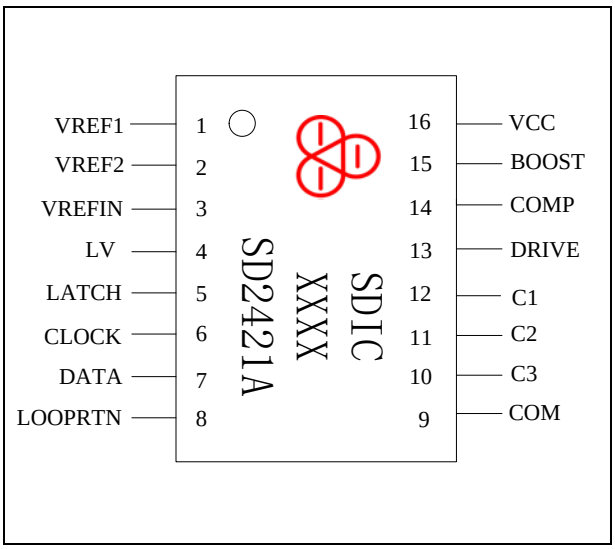



*Figure 1. Pin diagram*

Table 1. Pin Descriptions

| SOP | Pin Name | Attribute | Description |
|---|---|---|---|
| 1 | VREF1 | Analog output | 1.25V precision reference voltage output for other devices in the transmitter. Can source at least 0.5mA. Connect a 100kΩ resistor to COM if VREF1 needs to sink current (refer to “Precision Voltage Reference” section). |
| 2 | VREF2 | Analog output | 2.5V precision reference voltage output. Connects to VREFIN when SD2421 uses its own reference. Can be used by other devices in the transmitter. Can source at least 0.5mA. |
| 3 | VREFIN | Analog input | Reference voltage input that sets the output range of SD2421. Input should be 2.5V for normal operation. Can use SD2421’s own VREF2 or other external reference. |
| 4 | LV | Analog I/O | Voltage regulator output (VCC) control. Refer to Table 2 for connection choices. |
| 5 | LATCH | Digital input | DAC latch input. Rising edge loads data from the serial input shift register into the DAC latch, and hence updates the DAC output. Number of CLOCK cycles determines the DAC’s operation mode (refer to “Digital Interface” section). |
| 6 | CLOCK | Digital input | Data clock input. Rising edge loads DATA pin signal into input shift register. CLOCK cycle is the serial input bit rate, which can be as high as 3MHz. |
| 7 | DATA | Digital input | Digital data input to the serial input shift register. Data must be valid at CLOCK’s rising edge. |
| 8 | LOOPRTN | Analog output | Loop Return port where current flows out of SD2421 and returns to the current loop. |
| 9 | ACOM | Ground | Common ground reference for all analog input/output. |
| | DCOM | Ground | Common ground reference for all digital input/output, connect to ACOM for typical application. |
| 10 | C3 | Analog I/O | Capacitor port for the internal switching current source’s analog filter. Connect a low dielectric absorption capacitor to COM (e.g. ceramic cap). |
| 11 | C2 | Analog I/O | Capacitor port. Refer to C3 pin description. |
| 12 | C1 | Analog I/O | Capacitor port. Refer to C3 pin description. |
| 13 | DRIVE | Analog output | Voltage regulator drive output. Driving the external pass transistor to set up the desired VCC voltage. |
| 14 | COMP | Analog input | Voltage regulator compensation. Connect a 10nF cap to DRIVE to ensure stability of the regulator op amp/pass transistor loop. |
| 15 | BOOST | Analog input | Current input pin of the internal power transistor. Constitute big majority portion of the 4-20mA loop current. |
| 16 | AVCC | Power | Regulator/pass transistor voltage output. Power source for all analog of SD2421. Can also provide power to other devices in the smart transmitter system. Connect 2.2uF cap to COM. VCC value determined by LV connection. Refer to Table 2 for connection choices. |
| | DVCC | Power | Digital Power source of SD2421, connect to AVCC for typical application. |
| -- | NC | -- | -- |

## Circuit Description

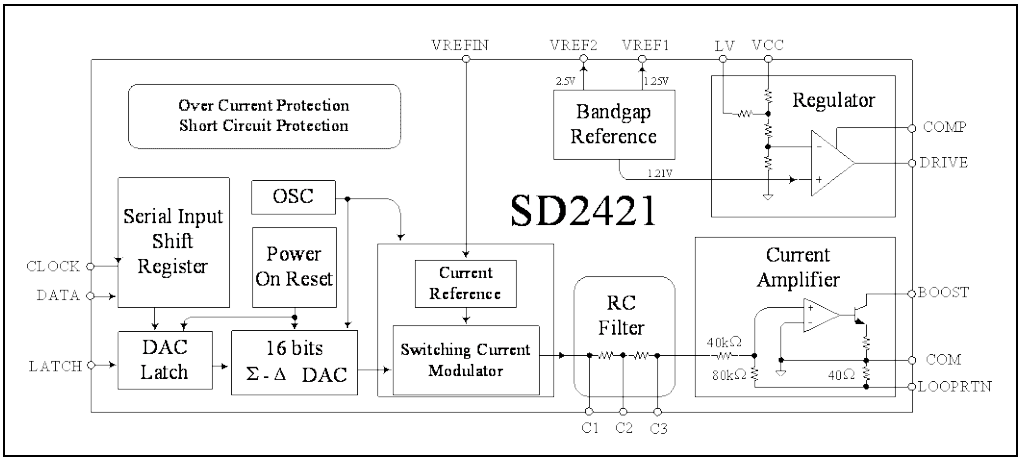



*Figure 2. Functional block diagram*

Figure 2 is the functional block diagram of SD2421. It is a 16 bits current DAC typically used in 4-20mA current loop powered smart transmitter. As a remote device, the transmitter receives its power from the current loop, and controls the current signal at the same time. SD2421 provides the following functions: DAC converting digital signal into analog current, current amplifier setting the loop current magnitude, and voltage regulator providing a stable operating voltage. Additionally, the IC has two accurate reference voltages, an internal oscillator, and high speed serial ports. Following are detail descriptions of major functional blocks.

### DAC

The SD2421 contains a 16 bits Σ-Δ DAC that converts the digital signal entering through the DATA pin into current. The DAC comprises a two stages modulator and an analog filter. The modulator's single bit output controls a switching current source. This current is then filtered by the analog filter.

The filter consists of two on chip resistors and three off chip capacitors between C1/C2/C3 and COM. The capacitors should have low dielectric absorption (NPO). The DAC's full scale settling time is determined by the filter. To realize 8ms setup time, the typical capacitor values should be C1=C2=10nF, and C3=3.3nF.

### Current Amplifier

Figure 3 shows the components in the current amplifier. It amplifies the DAC's filtered output and sets the current through the LOOPRTN pin. The DAC current flowing through the 80kΩ resistor forms the amplifier's input voltage. The amplifier/NPN feedback network sets the current through the 40Ω resistor (flowing in from BOOST and COM pins, and from the IC's internal COM node) to be 2000 times of the DAC current. The total loop current (flowing out of LOOPRTN) is 2001 times of the DAC current.

BOOST is normally connected to VCC, and the full 4-20mA loop current passes through the external FET. Refer to "Reducing External FET's Power Loading" section on how to lower the FET current.

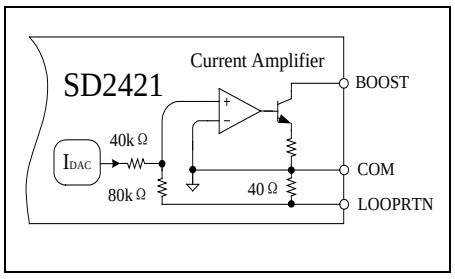



*Figure 3. Current amplifier circuit diagram*

## Voltage Regulator

The regulator consists of bandgap reference, op amp, and external depletion mode N channel FET. It provides VCC voltage to SD2421 itself and other devices in the transmitter. Figure 4 shows the connection that sets VCC to 3.3V.

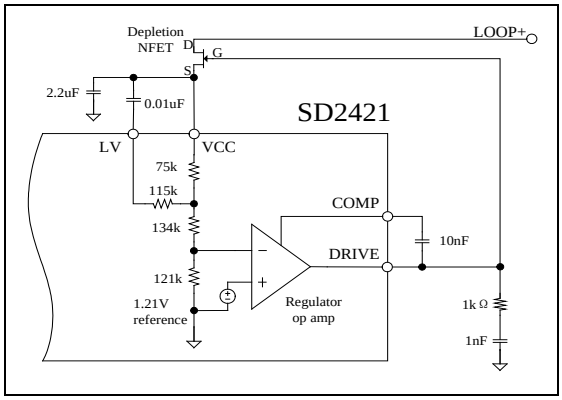



*Figure 4. Regulator circuit for 3.3V output*

Different VCC values can be obtained by changing the LV pin connection. Table 2 shows the relationship.

Table 2. LV Connection and VCC Output

| **LV connects to:** | **VCC** |
|---|---|
| COM | 5V |
| VCC or COM through 0.01uF cap | 3.3V |
| VCC | 3V |

The maximum loop voltage in the Figure 4 configuration is determined by the external NFET's breakdown and saturation voltages. The NFET should have suitable $V_{GS}$(off), $I_{DSS}$, and transconductance so that the regulator op amp's output at the DRIVE pin can correctly control the NFET's operating point while swinging between VCC and COM. Table 3 lists the key parameters when selecting the external FET. $V_{LOOP}$ is the loop voltage:

Table 3. FET Specification

| **FET type** | **N channel depletion type** |
|---|---|
| $I_{DSS}$ | 24mA (minimum) |
| $BV_{DS}$ | $V_{LOOP}$-VCC (minimum) |
| $V_{GS}$(off) | -VCC (maximum) |
| Minimum power | 24mA × ( $V_{LOOP}$-VCC) |

In order to ensure stable operation, the regulator requires some external resistor and capacitors for frequency compensation:

- 10nF cap between DRIVE and COMP
- 1kΩ resistor in series with 1nF cap between DRIVE and COM
- 2.2uF cap between VCC and COM

## Precision Voltage Reference

SD2421 has a built-in precision bandgap reference. It is used by the regulator loop. It also generates two reference voltages to be used by SD2421 and other external circuits. VREF1 is +1.25V and VREF2 is +2.5V. Both references can source 0.5mA currents.

Connect VREF2 to VREFIN if SD2421 uses its own voltage reference. Otherwise, connect an external voltage reference between VREFIN and COM.

To ensure stable operation, a 4.7uF cap must be connected between VREF2 and COM. If VREF1 is used by external circuits, a 4.7uF cap must also be connected between VREF1 and COM. This cap is not required if VREF1 is not used, but system noise can be lowered if it is connected.

VREF2 current is monitored by SD2421 continuously. If more than 0.5mA is drawn out by external circuits, the IC goes into power on reset. DAC is disabled, internal oscillator is stopped, and the input DATA latch is cleared.

VREF1 has limited current sinking capability. If current sink is needed, a 100kΩ resistor should be connected between VREF1 and COM.

### Digital Interface

SD2421 has three digital input ports: DATA, CLOCK, and LATCH. They can be connected to the microcontroller's serial ports directly. DATA is read MSB first into the shift register at the CLOCK's rising edge, and then loaded in parallel to the DAC latch at the LATCH's rising edge. The process is shown in Figure 5. Refer to Table 7 for the timing parameters.

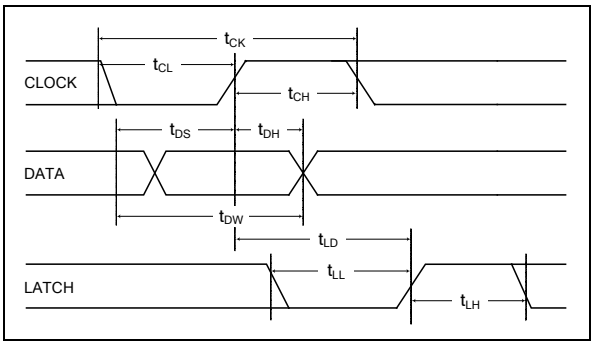



*Figure 5. Serial port timing diagram*

## Using the SD2421

SD2421 can be set for normal 4-20mA operation or alarm current operation. For normal operation, coding is 16 bits straight binary covering 4mA to 20mA range. For alarm current operation, coding is 17 bits covering 0mA to 32mA. User can set a value outside the normal 4-20mA range to indicate problem in the transducer.

To determine which operation is in effect, the number of CLOCK pulses between two consecutive LATCH rising edges is counted. 0-16 pulses imply normal operation. More than 16 pulses imply alarm current operation.

### 4-20mA Coding

Table 4 list the ideal relationship between input code and output current in normal operation. Resolution is 16 bits. VREFIN is +2.5V, 1LSB = 16mA/65536 = 244nA. If there are less than 16 CLOCK pulses between two consecutive LATCH rising edges, the missing DATA bits are by default set to 0.

Figure 6 shows the DATA input timing diagram for normal operation. In this figure, there are 16 CLOCK pulses between two consecutive LATCH rising edges. Input DATA is 88C3h. Output current is 12.547607mA.

Table 4. Ideal input/output code table for normal 4-20mA operation

| Input code | Output current |
|---|---|
| 0000 0000 0000 0000 | 4mA |
| 0000 0000 0000 0001 | 4.000244mA |
| 0100 0000 0000 0000 | 8mA |
| 1100 0000 0000 0000 | 16mA |
| 1111 1111 1111 1101 | 19.999268mA |
| 1111 1111 1111 1111 | 19.999756mA |

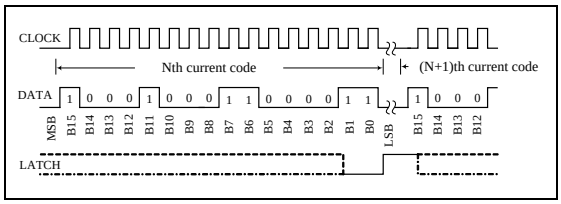



*Figure 6. DATA input timing diagram for normal operation*

### Alarm Current Coding

Table 5 list the ideal relationship between input code and output current in alarm current operation. Resolution is 17 bits. VREFIN is +2.5V, 1LSB = 32mA/131072 = 244nA. SD2421 only accepts the last 17 serial input DATA bits with LSB as the last bit. In other word, MSB is read at the 17$^{th}$ CLOCK rising edge before the LATCH rising edge.

In alarm current operation, the ideal output current range is 0mA to 32mA. However,

SD2421 cannot reliably generate current below 3.5mA or above 24mA. The user should set the code within those included in Table 5.

Table 5. Ideal input/output code table for alarm current operation

| Input code | Output current |
|---|---|
| 0 0011 1000 0000 0000 | 3. 5mA |
| 0 0100 0000 0000 0000 | 4mA |
| 0 1000 0000 0000 0000 | 8mA |
| 1 0000 0000 0000 0000 | 16mA |
| 1 0100 0000 0000 0000 | 20mA |
| 1 1000 0000 0000 0000 | 24mA |

Figure 7 shows an 8 bits microcontroller using three 8 bits write operations to set SD2421 into alarm current operation. Input DATA is 03A00h. Output current is 3.625mA.

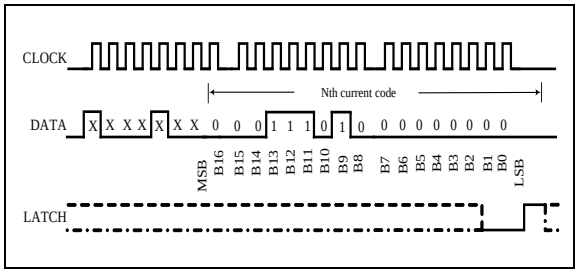



*Figure 7. DATA input timing diagram for current alarm operation*

## SD2421 –SPI Bus Interface

Figure 8 shows the typical SPI bus connection to SD2421. SPI's M_CLK and MOSI should connect to SD2421's CLOCK and DATA. The microcontroller needs to provide another IO port connecting to SD2421's LATCH input.

Figure 9 shows the typical SPI initialization and data transfer flow. SPI data port is set to 8 bits wide. Data is set to be sent at the clock's rising edge. An DIOn port is set as output.

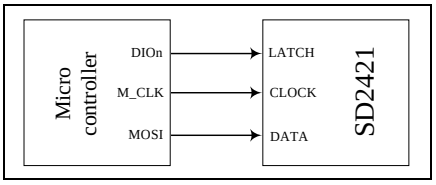



*Figure 8. SPI/SD2421 connection*

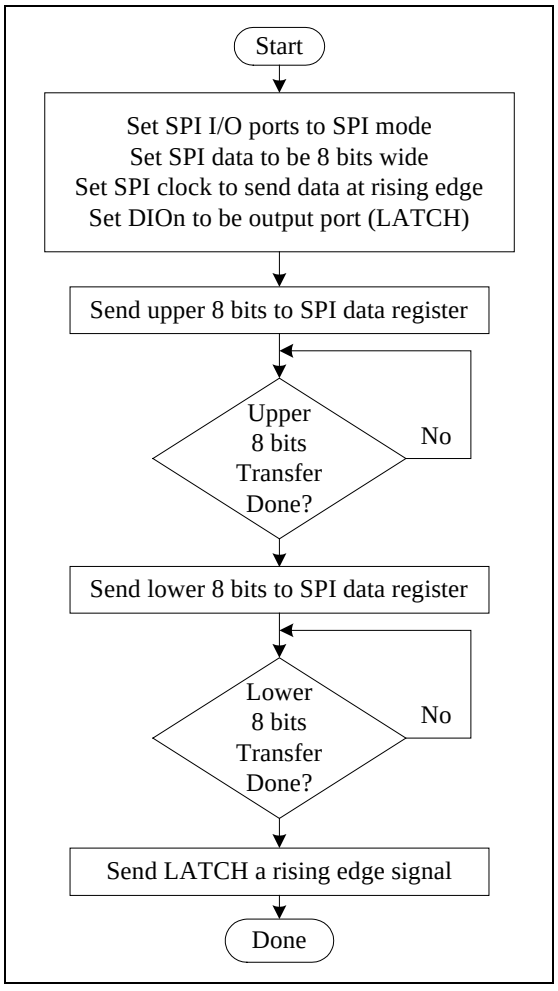



*Figure 9. Initialization and 16 bits code writing flow chart*

The microcontroller fetches the upper 8 bits from its memory and generates 8 clock pulses. Note that each data bit is valid at the clock's rising edge. After sending out the upper 8 bits, the microcontroller repeats the same steps for the lower 8 bits. Upon completion, the DIOn port sends a rising edge to complete the data sending procedure.

# Typical Applications

## Basic Operation Setup

Figure 10 shows a SD2421 application circuit at VCC=5V using minimum number of external components. SD2421 has very low VCC supply sensitivity. At 3V, 3.3V, and 5V supply, the typical loop current variation is 1nA/mV. This is far lower than other comparable products. Thus SD2421 does not require external resistor compensation for different VCC values.

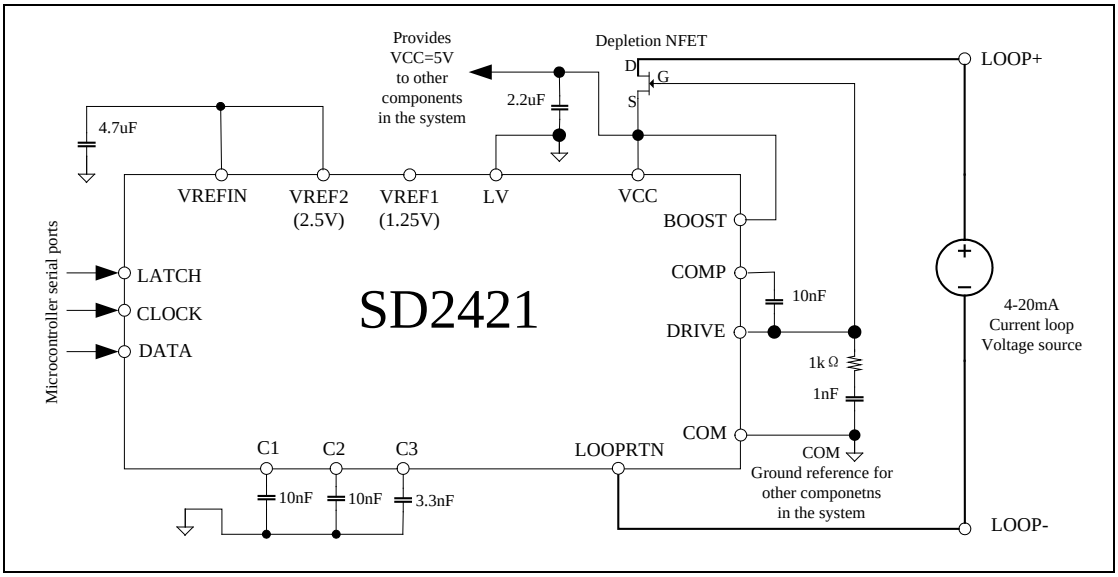



*Figure 10. Typical SD2421 application diagram*

## Reduce External FET's Power Loading

Figure 11 shows a circuit using external NPN transistor to lower the depletion FET's power requirement. Current going into the BOOST pin will come from the NPN. Current going into VCC will still come from the FET. The FET current can be lowered to 520uA (SD2421 own power consumption), or below 4mA (Other components in the system share power with VCC).

In this application, a 10nF cap must be connected between COM and LOOPRTN. The NPN must be able to sustain the maximum voltage between LOOP+ and LOOP-.

This circuit should be used only when the depletion FET does not have sufficient heat dissipation capacity or its $I_{DSS}$ is less or close to 24mA.

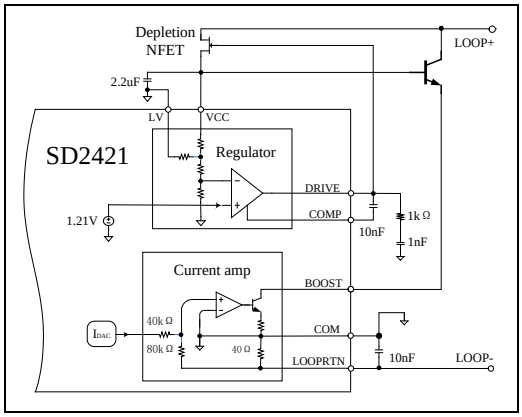



*Figure 11. External NPN lower FET's power burden*

## Smart Transducer

SD2421 is a current DAC specially designed for 4-20mA smart transducer. Figure 12 shows a typical application. Voltage signals from multiple transducers are converted into digital format by the ADC. The microcontroller reads the data, performing temperature compensation, linearization, or other signal processing, and then sends the data to SD2421 through the serial ports. SD2421 converts the digital data into current signal and send it to the control center through the 4-20mA loop.

SD2421 and the external depletion mode NFET together extract electric energy from the 4-20mA loop to provide a stable VCC voltage for the SD2421 itself and other devices in the transducer system.

In figure 12, the LV pin is connected to VCC through a 10nF capacitor. The resulting VCC is 3.3V.

VREF2 provides the reference voltage for SD2421 itself. VREF1 provides the reference voltage for the external ADC. One should connect a 4.7uF capacitor and 100kΩ resistor in parallel to COM.

In this example, the transducer does not have digital communication capability through the 4-20mA loop.

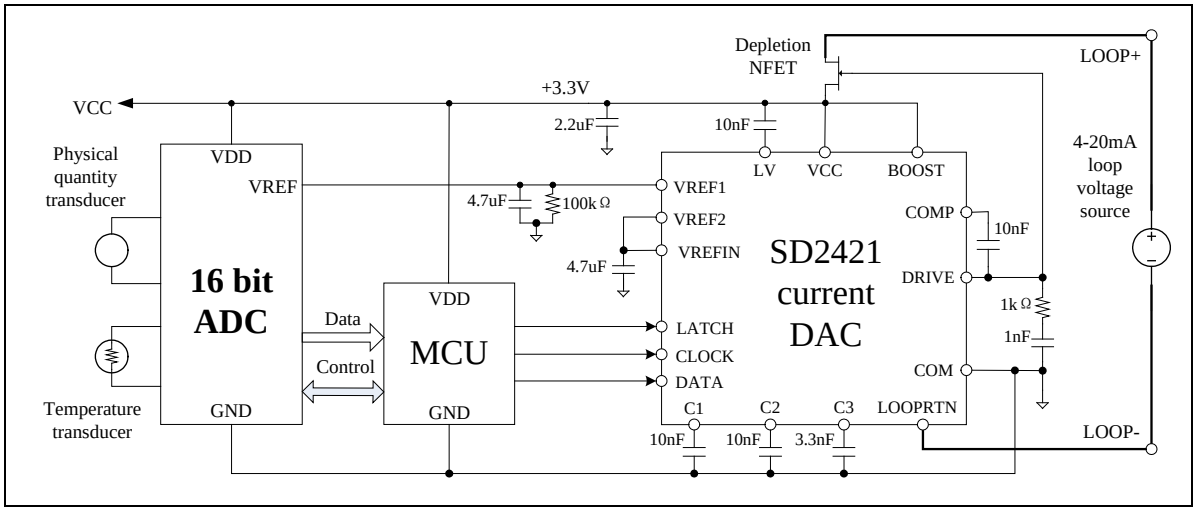



*Figure 12. Typical 4-20mA smart transducer without digital communication capability*

## HART Connection

HART protocol is a Frequency Shift Key(FSK) based digital communication standard. It uses 1200Hz and 2200Hz to represent the binary “1” and “0” as shown in figure 13. These $1mA_{pp}$, zero DC value sine waves are put on top of the 4-20mA current loop signal to allow simultaneous analog and digital communication. HART signal can easily be removed by a low pass filter, thus allowing pure analog instruments to work normally in a HART system. A 10Hz single pole low pass filter will reduce the HART signal to ±0.01% of the 20mA full scale signal.

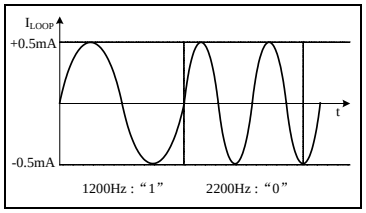



*Figure 13. HART signal*

Figure 14 shows a typical 4-20mA smart transducer with HART capability. HART signal comes in from the current loop at the LOOP+ terminal. It goes into the SD2015 HART modem through a discrete loop pass filter. SD2015 demodulates the signal and passes it to the MCU. To send HART signal out to the current loop, the MCU sends the logic data to SD2015 for modulation and wave shaping. The signal is then coupled to SD2421 through the Cc capacitor.

HART signal from SD2015 is capacitively attenuated by the $C_C$/C3 combination in order to have $1mA_{pp}$ current at the 4-20mA loop. Furthermore, according to HART protocol, a 25Hz double pole low pass filter is needed at the C3 pin. To implement the above requirements, $C_C$ should be 6.8nF, C2 should be 0.47uF, and C3 should be 0.15uF.

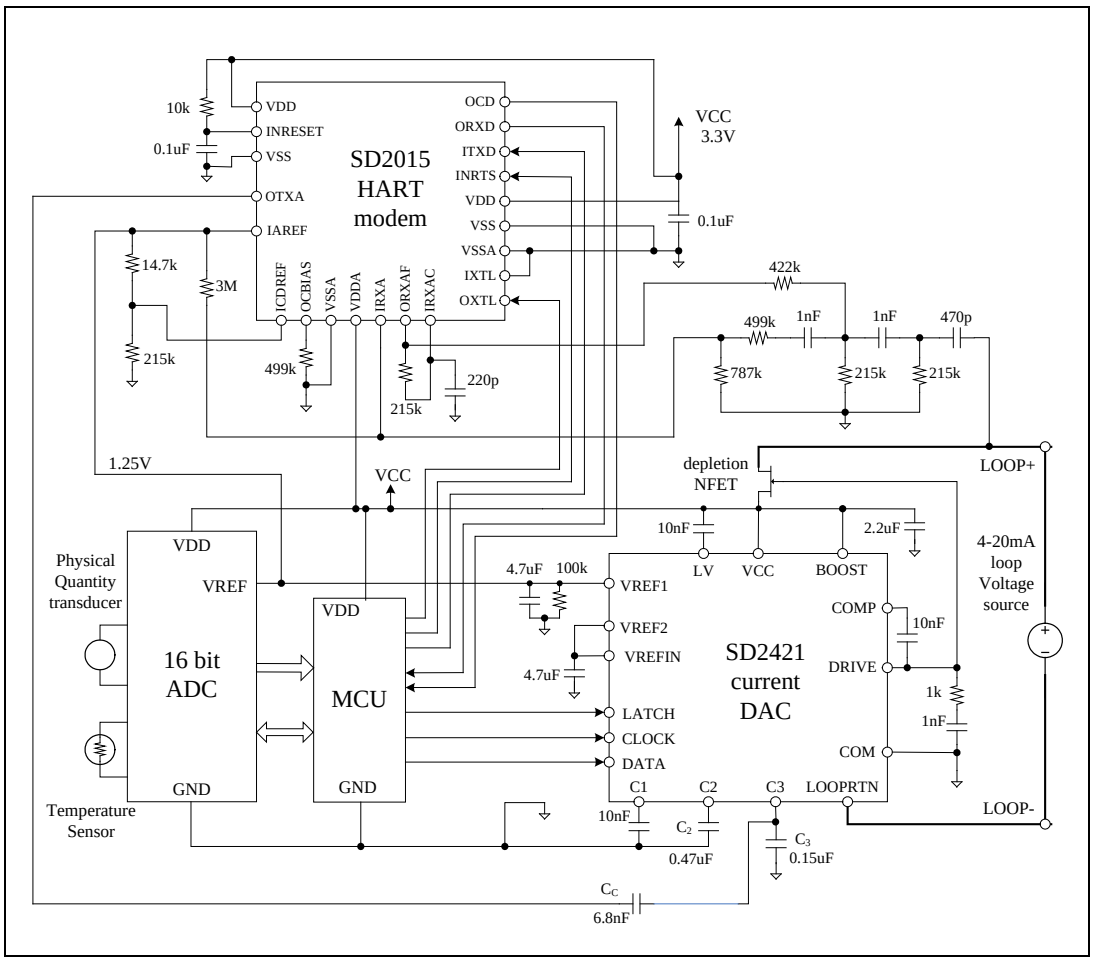



*Figure 14. Typical 4-20mA smart transducer With HART digital communication capability*

## Current Source

Figure 15 shows SD2421 being used as a current source. The 4-20mA current loop voltage source is local. Its current is adjusted by SD2421 based on the DATA signal. It is then output through Loop+, and returns back from Loop-. The remote load is usually resistive and across the Loop+/Loop- terminals.

In figure 15, the microcontroller and the 4-20mA loop are isolated by the opto-couplers. If these opto-coupler have long rise or fall time, Schmidt triggers should be used at the SD2421 input ports to stop false data from entering the DAC.

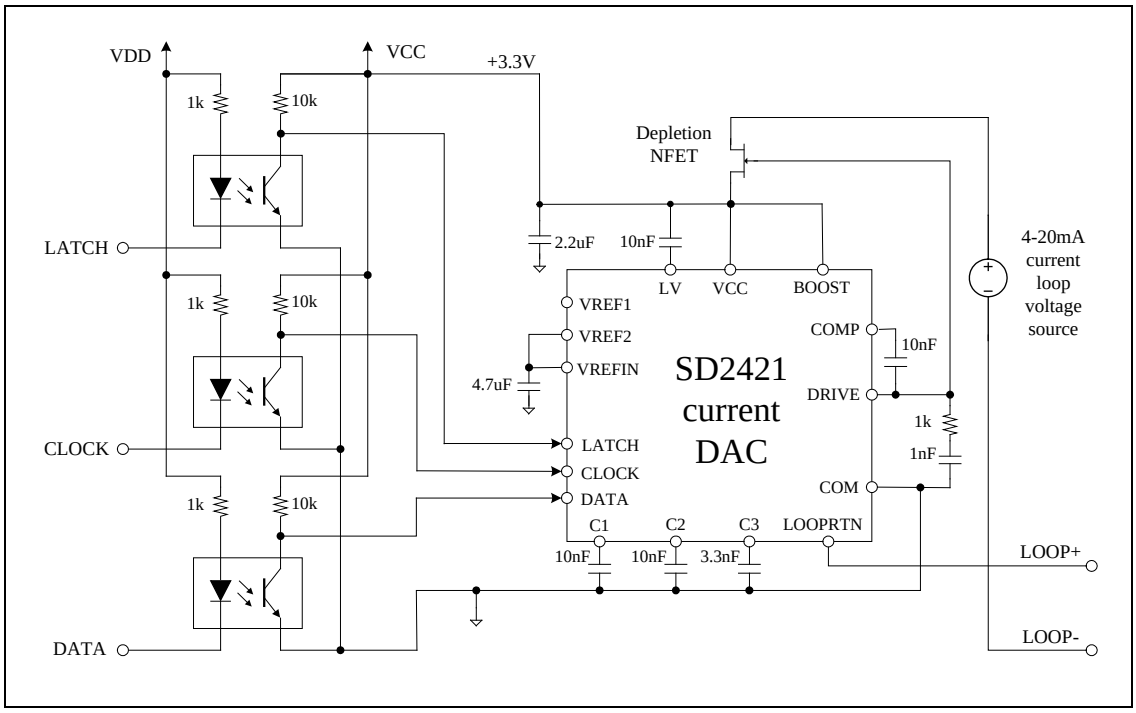



*Figure 15. Typical current source implementation*

## Battery Backup

Figure 16 shows a system where back up battery is used to power the microcontroller and memory during power outage. Thus data will be retained when VCC is lost due to current loop disconnect or some other reason. When VCC is working normally, the super capacitor or rechargeable battery is being charged through the PMOS transistor. R1, R2 values can be adjusted to provide the proper charging voltage. When VCC is lost, the PMOS gate voltage drops to 0V, current from the super capacitor or rechargeable battery can then flow through the PMOS channel and the body diode to provide power for the microcontroller and the memory.

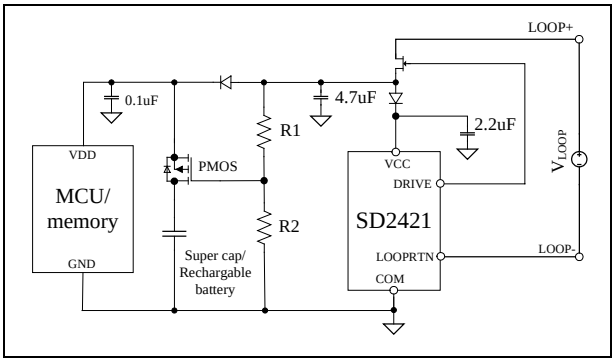



Figure 16. *Typical battery backup application*

## Electrical Specifications

Table 6. Absolute Maximum Ratings

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $T_A$ | Operating temperature | -40 | +85 | ℃ |
| $T_S$ | Storage temperature | -65 | +150 | ℃ |
| VCC to COM | Supply voltage | -0.3 | +7.0 | V |
| DRIVE, BOOST, COMP to COM | Analog input/output voltage | -0.3 | VCC+0.3 | V |
| LATCH, CLOCK, DATA to COM | Digital input/output voltage | -0.3 | VCC+0.3 | V |
| TL | Reflow temperature profile | Per IPC/JEDECJ-STD-020C | | ℃ |
| $\theta_{JA}$ | SOP16 thermo resistance | 110 | | ℃ /W |
| ESD | Human body model | 3500 | | V |
| | Machine model | 200 | | V |

Remarks:
1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and with care taken to not exceed the operating voltage range.
2. Turn off power before inserting or removing the device.

Table 7. Electrical Specifications
(VCC=3.0V ~ 5.0V, $T_A = T_{MIN} \sim T_{MAX}$, VREFIN=VREF2, Using DN2540 as external power device)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Conditions/Remarks |
|---|---|---|---|---|---|---|
| VCC | Supply voltage | 2.98 | 3 | 3.02 | V | |
| | | 3.28 | 3.3 | 3.32 | V | |
| | | 4.95 | 5 | 5.05 | V | |
| $Reg_{line}$ | Line regulation | | 1 | | uV/V | $\Delta VCC/\Delta V_{LOOP}$ |
| $Reg_{load}$ | Load regulation | | 150 | 200 | uV/mA | $\Delta VCC/\Delta I_{LOAD}$ |
| IDD | Supply current | | 400 | 480 | uA | VCC=3V |
| | | | 440 | 520 | uA | VCC=5V |
| | Loop voltage | VCC+2 | | | V | External depletion mode N-FET breakdown voltage |
| | Full scale settling time | | 8 | | ms | Settle to 99.9% C1=C2=10nF, C3=3.3nF |
| | Loop output resistance | | 100 | | MΩ | |
| | AC voltage sensitivity | | 0.5 | | uA/V | 1200Hz~2200Hz |
| | Loop inductive load | | 50 | | mH | See note 1 |
| DAC | | | | | | |
| | Resolution | | 16 | | Bits | |
| Vn | Current Noise | | 30<br>200 | | $nA_{rms}$<br>$nA_{p-p}$ | 4mA@25℃, VCC=5V<br>0.1Hz~10Hz |
| | | | 90<br>550 | | $nA_{rms}$<br>$nA_{p-p}$ | 20mA@25℃, VCC=5V<br>0.1Hz~10Hz |
| | Monotonicity | 16 | | | Bits | |
| INL | Integral Nonlinearity | | ±0.004 | ±0.01 | % FS | FS=Full scale output current |
| | Offset | | | ±0.02 | % FS | 4mA@+25℃,VCC=5V |
| | Offset drift | | ±10 | ±30 | ppm /℃ | Includes on-chip reference drift |
| | Total output error | | | ±0.1 | % FS | 20mA@+25℃,VCC=5V |
| | Total output drift | | ±10 | ±30 | ppm /℃ | Includes on-chip reference drift |
| | VCC supply sensitivity | | 1 | 3 | nA/mV | |

| | | | | | | |
|---|---|---|---|---|---|---|
| VREF2 | | | | | | |
| | Output voltage | 2.494 | 2.5 | 2.506 | V | |
| | Drift TC | | ±5 | ±10 | ppm /℃ | -40℃~+85℃ |
| | Output current | 0.5 | | | mA | |
| | VCC supply sensitivity | | 60 | 350 | uV/V | |
| | Output resistance | | 1 | | Ω | |
| | Noise | | 12 | | uVrms | 0.1Hz~10Hz |
| VREF1 | | | | | | |
| | Output voltage | 1.245 | 1.25 | 1.256 | V | 100kΩ load to COM |
| | Drift TC | | ±5 | ±10 | ppm /℃ | -40℃~+85℃ |
| | Output current | 0.5 | | | mA | |
| | VCC supply sensitivity | | 30 | 160 | uV/V | |
| | Output resistance | | 2 | | Ω | |
| | Noise | | 7.6 | | uVrms | 0.1Hz~10Hz |
| REF_IN | Input resistance | | 60 | | kΩ | |
| **Digital I/O parameter** | | | | | | |
| $V_{IH}$ | Input high voltage | 0.7*VCC | | | V | |
| $V_{IL}$ | Input low voltage | | | 0.3*VCC | V | |
| $I_{IH}$ | Input high current | | | ±0.5 | uA | $V_{IN}$ =VCC |
| $I_{IL}$ | Input low current | | | ±0.5 | uA | $V_{IN}$ =0V |
| | Data code | Binary | | | | |
| | Serial data rate | | | 3 | Mbps | |
| $t_{CK}$ | Data clock period | 320 | | | ns | |
| $t_{CL}$ | Data clock low time | 160 | | | ns | |
| $t_{CH}$ | Data clock high time | 160 | | | ns | |
| $t_{DW}$ | Data stable width | 160 | | | ns | |
| $t_{DS}$ | Data setup time | 80 | | | ns | |
| $t_{DH}$ | Data hold time | 80 | | | ns | |
| $t_{LD}$ | Latch delay time | 160 | | | ns | |
| $t_{LL}$ | Latch low time | 160 | | | ns | |
| $t_{LH}$ | Latch high time | 160 | | | ns | |

Note:

1. If using a serial inductor along the loop in order to suppress high frequency interference, one should connect a 0.1uF cap between the FET's drain and SD2421's LOOPRTN in order to guarantee system stability.

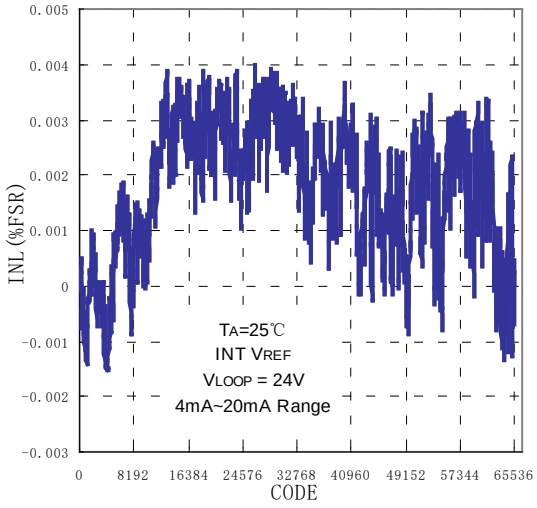



*Figure 17. INL vs. DAC Code*

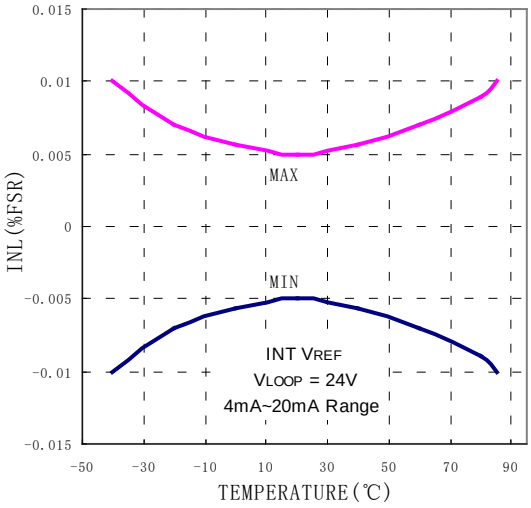



*Figure 18. INL vs. Temperature*

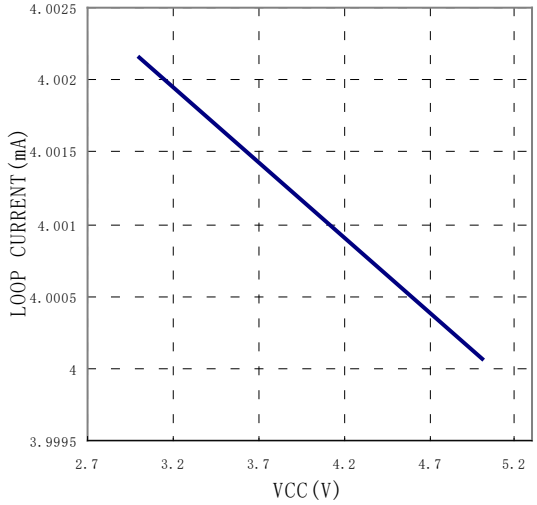



*Figure 19. Loop current vs. supply voltage*

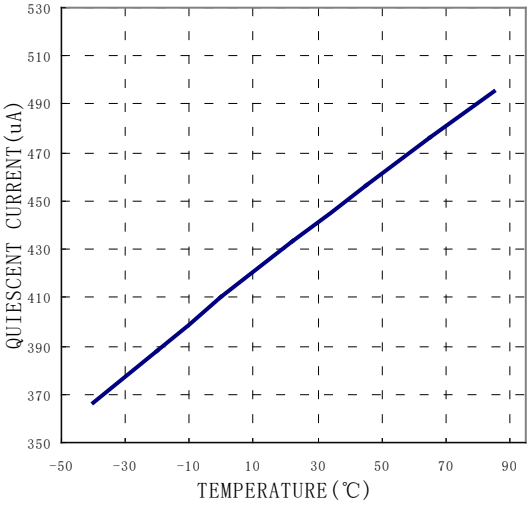



*Figure 20. Quiescent current vs. temperature (VCC=5V)*

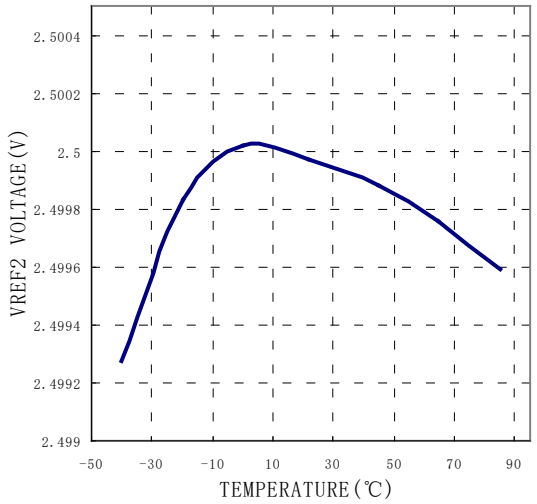



*Figure 21. VREF2 vs. temperature*

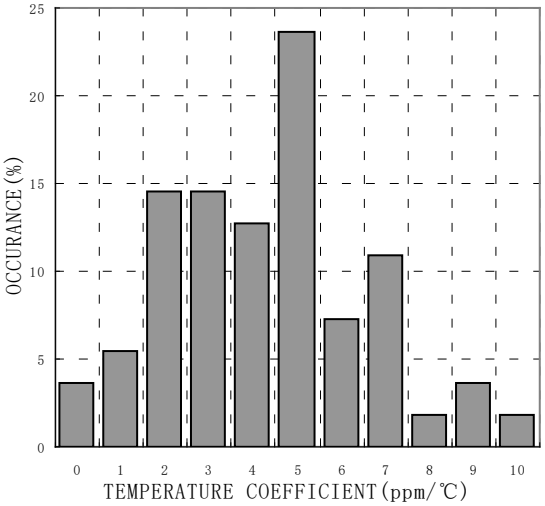
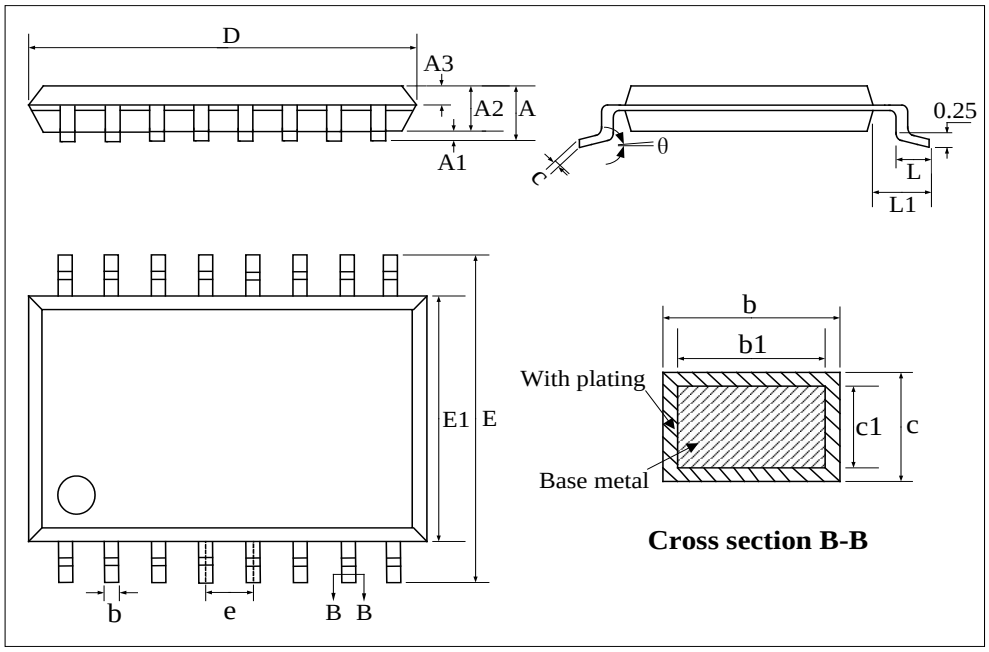



*Figure 22. VREF2 TC distributio*

## Packaging Information




*Dimensions: mm*

| Symbol | Min. | Nom. | Max. |
|---|---|---|---|
| A | — | — | 2.65 |
| A1 | 0.10 | — | 0.30 |
| A2 | 2.25 | 2.30 | 2.35 |
| A3 | 0.97 | 1.02 | 1.07 |
| b | 0.35 | — | 0.44 |
| b1 | 0.34 | 0.37 | 0.39 |
| c | 0.25 | — | 0.31 |
| c1 | 0.24 | 0.25 | 0.26 |
| D | 10.10 | 10.30 | 10.50 |
| E | 10.26 | 10.41 | 10.60 |
| E1 | 7.30 | 7.50 | 7.70 |
| e | 1.27BSC | | |
| L | 0.55 | — | 0.85 |
| L1 | 1.40BSC | | |
| θ | 0.00 | — | 8° |

*Figure 23. SOP16(wide body) mechanical specification*