SD2017
Low Power HART™ Modem

Feature

- Meets HART physical layer requirements
- Single chip, half duplex 1200 bps FSK modem
- Bell 202 shift frequencies of 1.2kHz and 2.2kHz
- Buffered HART output for drive capability
- External 3.6864MHz crystal or clock source
- 2.7V to 5.5V power supply
- 90μA maximum supply current in transmit mode
- -55 ℃ to +125 ℃ operation range
- 32 pin LQFP packages
- RoHS compliant

General Description

The SD2017 is a CMOS single chip modem IC used in Highway Addressable Remote Transducer (HART) field instruments and masters. This IC together with a few external passive components provide all functions needed to satisfy HART physical layer requirements including modulation, demodulation, receive filtering, carrier detect, and transmit signal wave shaping.

The SD2017 uses phase continuous Frequency Shift Keying (FSK) at 1200 bps, and operates in half duplex mode per HART protocol. The maximum supply current consumption in transmit mode is 90μA while using 3.6864MHz external Clock source input and 5.5V power supply.

The SD2017 is pin compatible with SD2015, HT2015 and A5191HRT. There is no need to change PCB when replacing any of the above ICs with SD2017. Some components on the original PCB are no longer needed, while others are changed to different types or different values. Refer to “Replacing SD2015 with SD2017” section for details.

Ordering Information

Package	Part Number
LQFP32 (7mm x 7mm)	SD2017B

Pin Diagram and Descriptions

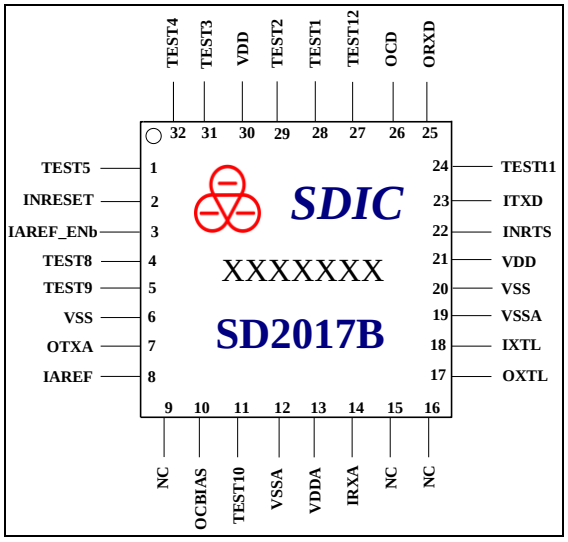


Figure 1. LQFP32 Pin diagram

Table 1. Pin Descriptions

Pin Name	Attribute	LQFP	Description
TEST1	-	28	No Connect or connect to VSS.
TEST2	-	29	No Connect or connect to VSS.
TEST3	-	31	No Connect or connect to VSS.
TEST4	-	32	No Connect or connect to VSS.
TEST5	-	1	Connect to VSS.
INRESET	Digital input	2	Reset all digital logic, active low.
IAREF_ENb	Digital input	3	Reference enable. A low state enables the internal 1.5V reference and buffer. A high stage disables the internal reference and input buffer, and a buffered external 2.5V reference source must be applied at IAREF.
TEST8	-	4	Connect to VSS.
TEST9	-	5	Connect to VSS.
OTXA	Analog output	7	HART FSK signal output. Connect to 4-20mA loop interface circuit.
IAREF	Analog output	8	Internal 1.5V reference voltage output. Connect a 1μF capacitor to VSSA.
NC	-	9	No Connect or connect to VSS.
OCBIAS	Analog output	10	Circuit bias current setting.
TEST10	-	11	No Connect or connect to VSS.
VDDA	Analog power	13	Analog supply voltage, same voltage level with VDD.
IRXA	Analog input	14	FSK modulated HART signal received from 4-20mA loop interface circuit.
NC	-	15	No Connect or connect to VSS.
NC	-	16	No Connect or connect to VSS.
OXTL	Analog output	17	Crystal oscillator output.
IXTL	Analog input	18	Crystal oscillator input.
VSS	Digital gnd	6,20	Digital ground, same voltage level with VSSA.
VDD	Digital power	21,30	Digital supply voltage, same voltage level with VDDA.
INRTS	Digital input	22	Request to sent, active low.
ITXD	Digital input	23	Data to be transmitted. After modulation, data goes out at OTXA.
TEST11	-	24	No Connect or connect to VSS.
ORXD	Digital output	25	Demodulated HART data, output to external UART.
OCD	Digital output	26	Carrier detect, high when data valid at IRXA.
TEST12	-	27	No Connect or connect to VSS.
VSSA	Analog gnd	12,19	Analog ground, same voltage level with VSS.

Circuit Description

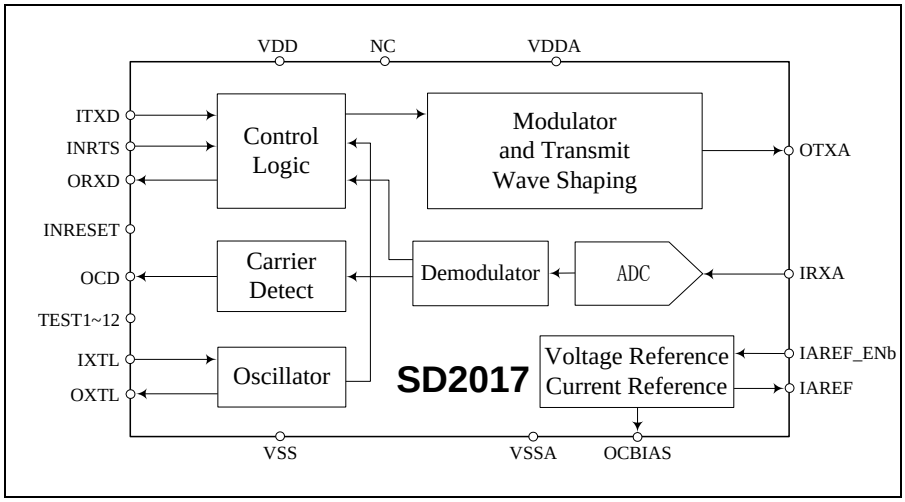


Figure 2. Function block diagram

Figure 2 is the function block diagram of SD2017. It is a low power HART FSK half duplex single chip modem that compiles with HART physical layer requirements. SD2017 includes the modulator and wave shaper for transmitting data; and includes the ADC, demodulator, and carrier detect circuitry for receiving data. Other functional blocks include reference voltage, crystal oscillator, and current reference.

The SD2017 transmits or receives 1200Hz and 2200Hz FSK signals. 1200Hz represents digital "1", whereas 2200Hz represents digital "0". The bit rate is 1200bits/second.

The oscillator provides time base for the modem using either 3.6864MHz external crystal or 3.6864MHz external clock source.

Modulator and Wave Shaping

When INRTS is set to low, the SD2017 operates in transmit mode. The modulator converts the NRZ digital signals at ITXD into a sequence of phase continuous 1200Hz and 2200Hz HART compliant trapezoidal signals through the wave shaping block. The signals are then output to OTXA as shown in Figure 3 and Figure 4. The OTXA DC level is 0.75V with 0.5V~1.0V voltage swing.

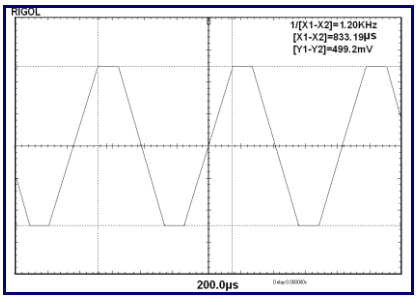


Figure 3. OTXA at logic 1 (1200Hz)

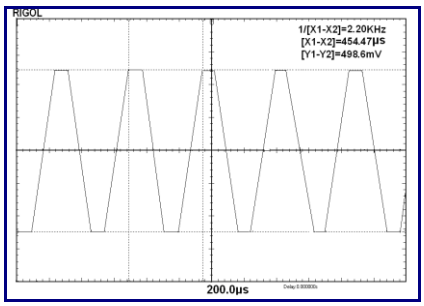


Figure 4. OTXA at logic 0 (2200Hz)

OTXA can drive capacitive load directly. The load should be 4.7nF to 68nF. SD2017 consumes more current as the capacitive load increases. The supply current specifications shown in Table 3 are based on a 4.7nF capacitive load at OTXA.

If driving a load with resistive element, it

should be coupled with a 2.2μF serial capacitor as shown in Figure 5. The R_{LOAD} range is typically 200Ω to 600Ω. A 22nF capacitor should be connected between OTXA and ground.

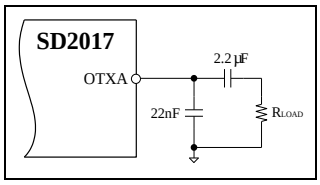


Figure 5. OTXA with resistive load

Demodulator and Carrier Detect

When INRTS is set to high, the SD2017 operates in receive mode. HART signal goes into IRXA through an external anti-aliasing band-pass filter. A high on OCD indicates a valid carrier is detected. The demodulator accepts the FSK signal at IRXA and restores to digital signal at ORXD, which is then output to external UART. The nominal bit rate is 1200 bps. Figure 6 illustrates the demodulation process.

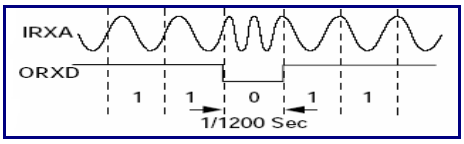


Figure 6. Demodulator signal timing

The carrier detect circuit determines whether the carrier's amplitude at IRXA meets the HART protocol requirement, and outputs the result at OCD. When OCD output is high, the modulator outputs the demodulated digital data at ORXD.

The demodulated digital data will appear at ORXD only after the carrier detect circuit decided that signals at IRXA are large enough to be detected (105mVp-p typically). According to HART specification, at 3.6864MHz (±1.0%) clock frequency and zero input (IRXA) asymmetry, the maximum demodulator jitter is less than 12% of one ORXD output bit.

The carrier detect set the carrier detect output pin OCD to logic 1 if INRTS is logic 1 and four consecutive pulses out of the comparator have arrived. OCD stays logic 1 as long as INRTS is logic 1 and the next comparator pulse is received in less than 2.5ms.

Once OCD goes inactive (logic 0), it takes another four consecutive pulses out of the comparator to assert OCD again.

Receiving Filter for Demodulator

The external band-pass filter is shown in Figure 7. A 200kΩ resistor at the filter input limits current to a sufficiently low level resulting in very high transient voltage protection capability. Therefore, no additional protection circuitry at the input terminal is needed even in the most demanding industrial environments. Using 1% accuracy resistor and 10% accuracy capacitor, effect of the filter on the carrier detection is still negligible.

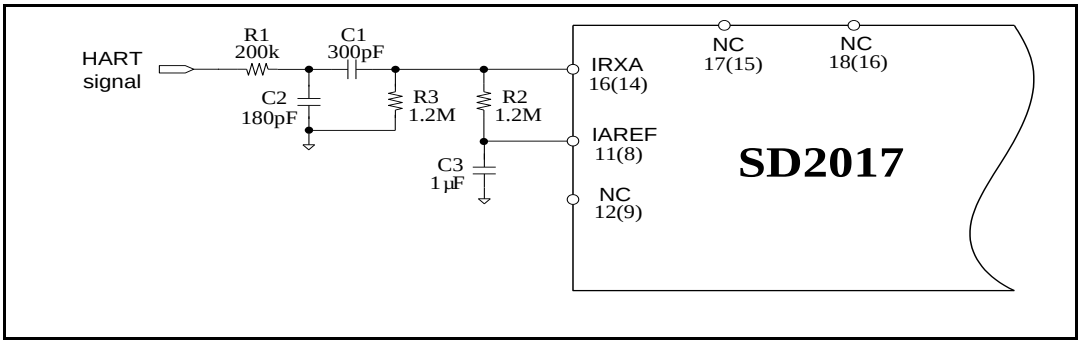


Figure 7. SD2017 external filter connection

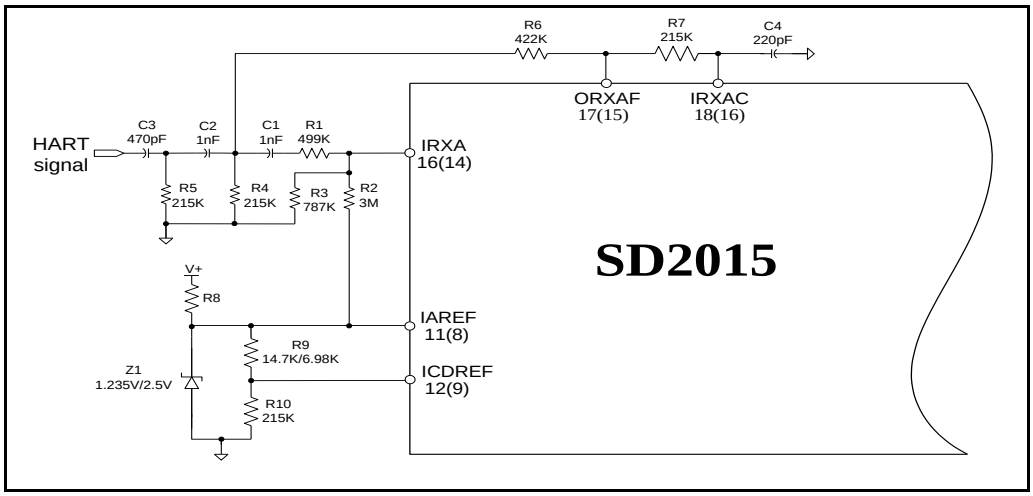


Figure 8. SD2015 external filter connection

Replacing SD2015 with SD2017

SD2017 can replace SD2015 directly because their pins are compatible. There is no need to modify the PCB. Some external components are removed, and some resistance and capacitance values and types are changed. Referring to Figure 8, the following list includes all external component modifications needed on the PCB when replacing SD2015 with SD2017.

- Remove C4, R7, R6, R5, R8 and Z1
- Change R1, R10 and C3 to 0Ω resistor
- Modify R2 and R3 to 1.2MΩ resistor
- Change C2 to 200kΩ resistor
- Modify C1 to 300pF capacitor
- Change R4 to 180pF capacitor
- Change R9 to 1μF capacitor

In addition, replace the 460.8kHz clock source with a 3.6864MHz clock source. Refer to "Clock Configuration" section for more details.

Bias Current Resistor

A resistor RBIAS is needed between OCBIAS and VSSA in order to create the bias current IOCB (IOCB=VIAREF/RBIAS). This bias current controls the operating point of internal functional blocks. It should be set to approximately 4.5μA. Since typical VIAREF is 1.5V, the recommended RBIAS value is 330KΩ.

Clock Configuration

The SD2017 provides two clocking options: external crystal and CMOS clock input.

The typical connection for the external 3.6864MHz crystal is shown in Figure 9. The crystal and capacitor should be as close to SD2017 as possible.

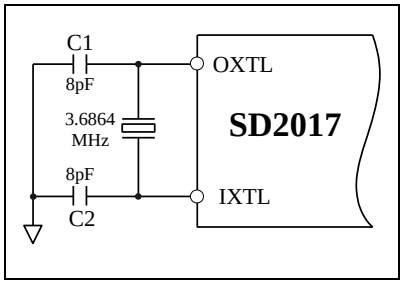


Figure 9. Crystal oscillator connection

The typical connection of CMOS clock input is shown in Figure 10 where an external 3.6864MHz clock source is connected to OXTL. IXTL should connect to ground.

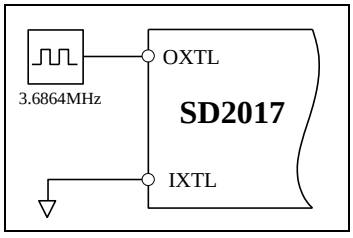


Figure 10. CMOS clock connection

Using the SD2017

Typical Application Diagram

Figure 11 is a typical smart transducer with HART capability using SD2017 and SD2421 (4-20mA loop-powered DAC). Decouple the power supplies with 1μF and 0.1μF capacitors in parallel to ground, and decouple the REF pin with a 1μF capacitor to ground.

HART signal comes in from the current loop's LOOP+ terminal, and goes into SD2017's IRXA pin through the external band-pass filter. SD2017 demodulates the signal and passes the digital data to the MCU through the ORXD pin.

To send HART signal out to the current loop, the MCU sends digital data to SD2017's ITXD pin. SD2017 performs modulation and wave shaping, and send the HART signal out through its OTXA pin and the Cc capacitor to SD2421's C3 pin. SD2421 then passes the signal to the current loop.

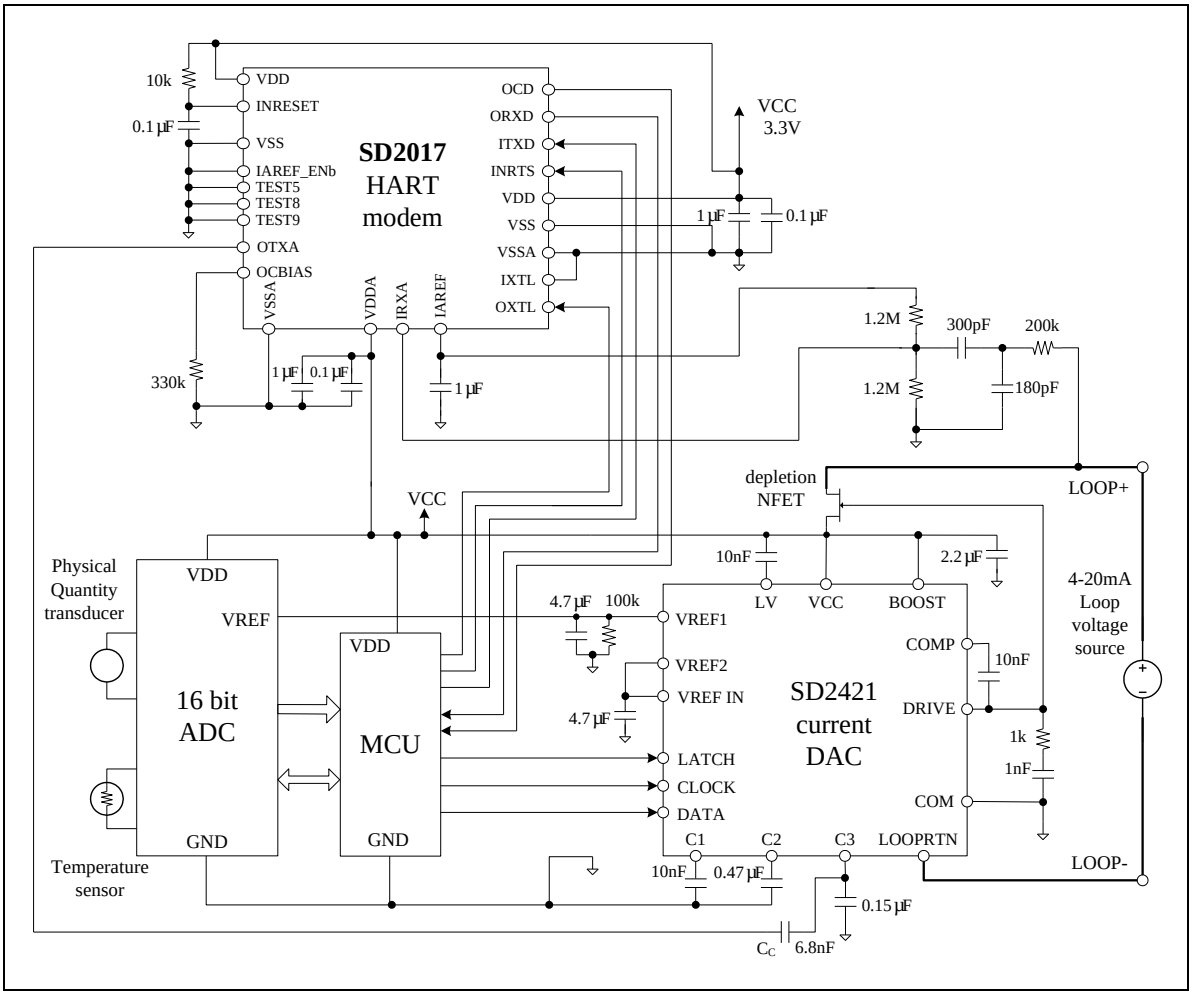


Figure 11. Typical 4-20mA smart transducer with HART digital communication capability

Electrical Specifications

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-55	+125	℃
T_S	Storage temperature	-65	+150	℃
VDDA，VDD	Supply voltage	-0.3	+7.0	V
V_{IN}，V_{OUT}	Input/output voltage	-0.3	VDD+0.3 or +7 (whichever is less)	V
TL	Reflow temperature profile		Per IPC/JEDECJ-STD-020C	℃
ESD	Human body model	4000		V
	Machine model	400		V

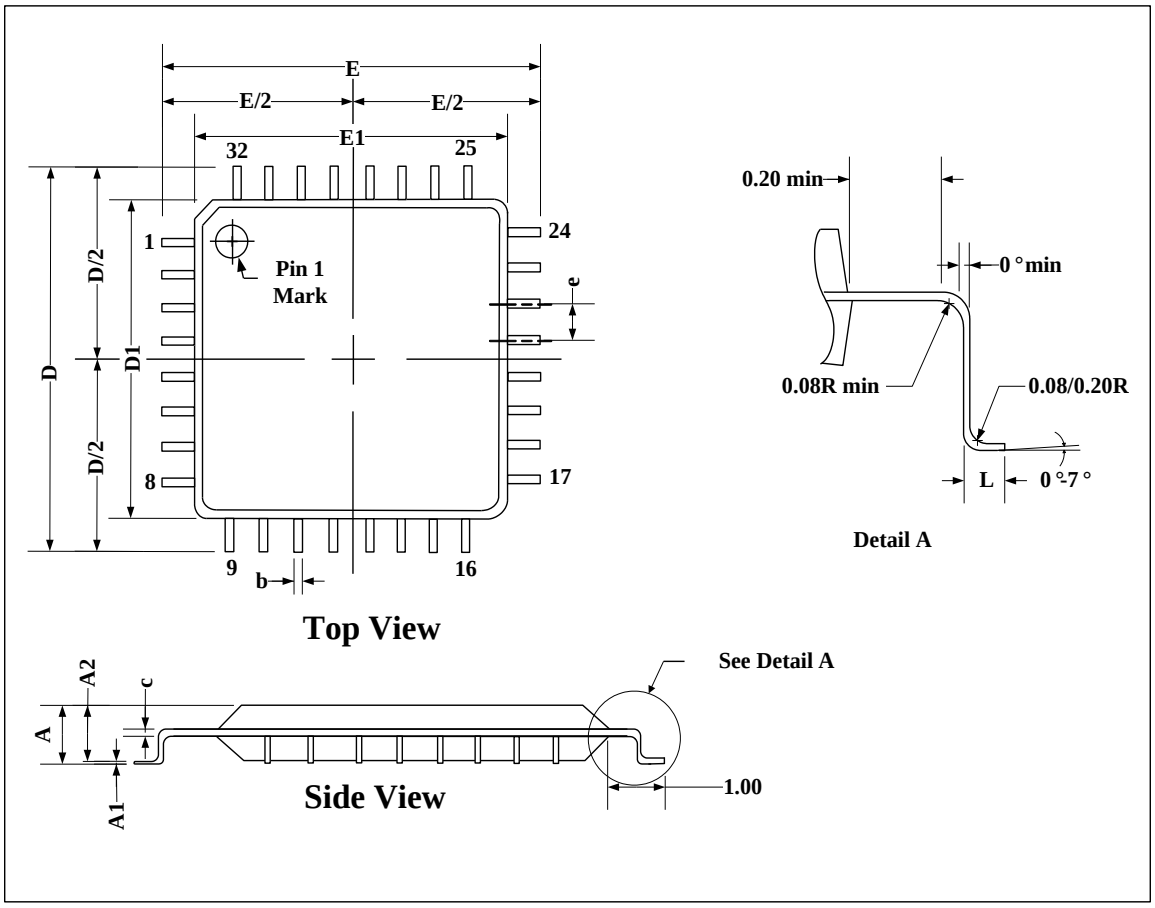
Remarks:

1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and with care taken to not exceed the operating voltage range.
2. Turn off power before inserting or removing the device.

Table 3. Electrical Specifications (VDDA=VDD=+2.7V~+5.5V, T_A=-55℃~+125℃, VSSA=VSS=0V, external crystal, 8pF at IXTL/OXTL, OXTA with 4.7nF load, unless otherwise noted)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
VDDA VDD	Supply voltage	2.7	3.3	5.5	V	
IDD	VDDA+VDD Demodulator mode		97	135	μA	External clock, -55℃ to +85℃
				140	μA	External clock, -55℃ to +125℃
			150	220		External crystal, -55℃ to +85℃
				240		External crystal, -55℃ to +125℃
	VDDA+VDD Modulator mode		67	85	μA	External clock, -55℃ to +85℃
				90	μA	External clock, -55℃ to +125℃
			112	175		External crystal, -55℃ to +85℃
				190		External crystal, -55℃ to +125℃
V_{IAREF}	Initial accuracy	1.48	1.5	1.52	V	
	Load regulation		1.5		ppm/μA	Tested with 500μA load
	Line regulation		60		μV/V	
I_{OCB}	Bias current		4.5		μA	
OCD assert	Carrier amplitude	90	105	115	mVp-p	
IRXA	Input voltage range	0		1.5	V	
OTXA	Output amplitude		500		mVp-p	
	“1” frequency		1200		Hz	
	“0” frequency		2200		Hz	
	Phase error			0	°	
	Maximum resistive load		160		Ω	R_{LOAD} shown in Figure5
External clock	Frequency accuracy	3.6496	3.6864	3.7232	MHz	
Digital I/O parameter						
V_{IH}	Input high voltage	0.7*VDD			V	
V_{IL}	Input low voltage			0.3*VDD	V	
I_{IH}	Input high current			±0.1	μA	
I_{IL}	Input low current			±0.1	μA	

Packaging Information



Dimension: mm

Symbol	Min.	Nom.	Max.
A	—	—	1.6
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	—	9.00	—
D/2	—	4.50	—
D1	—	7.00	—
E	—	9.00	—
E/2	—	4.50	—
E1	—	7.00	—
L	0.45	0.60	0.75
e	—	0.80	—
b	0.30	0.37	0.45
c	0.09	—	0.20

Figure 12. LQFP32 mechanical specification